WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate including opposed first and second surfaces and a recess which is depressed in a direction from the first surface to the second surface, the first surface including the recess being covered with an insulating film;

pads formed on the insulating film at a bottom surface of the recess;

first external terminals formed on the insulating film on the first surface at an area surrounding the recess;

wiring formed on the insulating film on the first surface for electrically connecting the pads to the first external terminals;

a first semiconductor element including a third surface, on which second external terminals are formed, and a fourth surface opposed to the third surface, the first semiconductor element being accommodated in the recess and the second external terminals being electrically connected to the pads;

a second semiconductor element including a fifth surface, on which third external terminals are formed, and a sixth surface opposed to the fifth surface, the second semiconductor element being accommodated in the recess and the sixth surface thereof being adhered to the fourth surface of the first semiconductor element.

2. The semiconductor device according to claim 1, wherein the substrate is a metal substrate.

3. The semiconductor device according to claim 1, wherein the third external terminals are disposed at the same height as the first external terminals.

4. The semiconductor device according to claim 1, wherein a stepped area is formed in the recess of the substrate, the second semiconductor element is accommodated in the recess and the sixth surface thereof is fixed to the fourth surface and the stepped area, and the third external terminals are disposed at the same height as the first external terminals.

5. A semiconductor device comprising:

an insulative substrate including opposed first and second surfaces and a recess having predetermined dimensions formed in the first surface;

pads formed at a bottom surface of the recess;

first external terminals formed on the first surface at an area surrounding the recess;

wiring formed on the substrate for electrically connecting the pads to the first external terminals;

a first semiconductor element including a third surface, on which second external terminals are formed, and a fourth surface opposed to the third surface, the first semiconductor element being

accommodated in the recess and the second external terminals being fixed to the pads; and

a second semiconductor element including a fifth surface, on which third external terminals are formed, and a sixth surface opposed to the fifth surface, the second semiconductor element being accommodated in the recess, the sixth surface thereof being fixed to the fourth surface, and the third external terminals being disposed at the same height as the first external terminals.

6. A semiconductor device comprising:

an insulative substrate including opposed first and second surfaces and a recess having predetermined dimensions formed in the first surface;

pads formed at a bottom surface of the recess;

first internal connection terminals formed on the first surface at an area surrounding the recess;

first external terminals formed on the first surface at outer sides than the first internal connection terminals;

wiring formed on the substrate for electrically connecting the pads to the first internal connection terminals and the first external terminals;

a first semiconductor element including a third surface, on which second external terminals are formed, and a fourth surface opposed to the third surface, the first semiconductor element being

accommodated in the recess and the second external terminals being fixed to the pads; and

a second semiconductor element including a fifth surface, on which third external terminals are formed and second internal connection terminals are formed in the vicinity of an outer edge at outer sides than the third external terminals, and a sixth surface opposed to the fifth surface, the second semiconductor element being accommodated in the recess, the sixth surface thereof being fixed to the fourth surface, the second internal connection terminals being electrically connected to the first internal connection terminals, and the third external terminals being disposed at the same height as the first external terminals.

7. The semiconductor device according to claim 5, wherein the wiring comprises a first wiring body formed at the bottom surface of the recess and electrically connected to the pads, a second wiring body formed on the first surface at an area surrounding the recess and electrically connected to the first external terminals, and a through hole formed in the substrate for electrically connecting the first wiring body to the second wiring body.

8. The semiconductor device according to claim 6, wherein the wiring comprises a first wiring body formed at the bottom surface of the recess and electrically connected to the pads, a second wiring body formed on the first surface at an area surrounding the recess and

electrically connected to the first internal connection terminals and the first external terminals, and a through hole formed in the substrate for electrically connecting the first wiring body to the second wiring body.

9. The semiconductor device according to claim 5, wherein the substrate comprises a first insulative substrate body and a second insulative substrate body, the second insulative substrate body including an opening, which forms the recess, and being fixed to a back surface of the first substrate body.

10. The semiconductor device according to claim 6, wherein the substrate comprises a first insulative substrate body and a second insulative substrate body, the second insulative substrate body including an opening, which forms the recess, and being fixed to a back surface of the first substrate body.

11. The semiconductor device according to claim 5, wherein a clearance between a wall surface of the recess and the first and second semiconductor elements is sealed with a sealing body.

12. The semiconductor device according to claim 6, wherein a clearance between a wall surface of the recess and the first and second semiconductor elements is sealed with a sealing body.

13. The semiconductor device according to claim 5, further comprising a heat sink fixed at the second surface of the substrate.

14. The semiconductor device according to claim 6, further comprising a heat sink fixed at the second surface of the substrate.

15. The semiconductor device according to claim 1, wherein the first semiconductor element comprises a wafer level chip size package where the second external terminals are arranged planarly by rewiring from internal electrodes provided with an insulating coating, and the second semiconductor element comprises a wafer level chip size package where the third external terminals are arranged planarly by rewiring from internal electrodes provided with an insulating coating.

16. The semiconductor device according to claim 5, wherein the first semiconductor element comprises a wafer level chip size package where the second external terminals are arranged planarly by rewiring from internal electrodes provided with an insulating coating, and the second semiconductor element comprises a wafer level chip size package where the third external terminals are arranged planarly by rewiring from internal electrodes provided with an insulating coating.

17. The semiconductor device according to claim 6, wherein the first semiconductor element comprises a wafer level chip size package where the second external terminals are arranged planarly by rewiring

from internal electrodes provided with an insulating coating, and the second semiconductor element comprises a wafer level chip size package where the third external terminals are arranged planarly by rewiring from internal electrodes provided with an insulating coating.